WE CLAIM:

1. An apparatus, comprising:

a current source circuit that is arranged to provide current from a first node to a second node, wherein the first node is associated with a local power supply, and wherein the second node is associated with a reference signal;

a controlled current source circuit that is arranged to selectively sink current from the second node to a third node in response to a control signal from a fourth node, wherein the third node is associated with a signal ground;

a band-gap core circuit that is coupled between the second node and the third node, wherein the band-gap core is arranged to provide a first sense signal to a fifth node and a second sense signal to a sixth node; and

an amplifier circuit, wherein the amplifier circuit includes a first input that is coupled to the fifth node, a second input that is coupled to the sixth node, and an output that is coupled to the fourth node.

2. The apparatus of Claim 1, wherein the amplifier circuit includes an input stage, wherein the input stage includes at least one of an n-type transistor pair, a p-type transistor pair, a FET type transistor pair, and a BJT type transistor pair.

3. The apparatus of Claim 1, the amplifier circuit comprising:

a first transistor that includes an emitter that is coupled to an eight node, a base that is coupled to the fifth node, and a collector that is coupled to the fourth node;

a second transistor that includes an emitter that is coupled to the eight node, a base that is coupled to the sixth node, and a collector that is coupled to an intermediary node;

a third current source that is coupled between the first node and the eight node; and

a current mirror that includes a first terminal that is coupled to the fourth node, a second terminal that is coupled to the intermediary node, and a third terminal that is coupled to the signal ground.

4. The apparatus of Claim 3, further comprising:

a first cascode transistor that includes a source that is coupled to the collector of the first transistor, a gate that is coupled to a bias signal, and a drain that is coupled to the fourth node such that the first transistor is coupled to the fourth node through the first cascode transistor; and

a second cascode transistor that includes a source that is coupled to the collector of the second transistor, a gate that is coupled to the bias signal, and a drain that is coupled to the intermediary node such that the second transistor is coupled to the current mirror through the second cascode transistor;

5. The apparatus of Claim 1, the amplifier circuit comprising:

a first transistor that includes a source that is coupled to an eight node, a gate that is coupled to the fifth node, and a drain that is coupled to the fourth node;

a second transistor that includes a source that is coupled to the eight node, a gate that is coupled to the sixth node, and a drain that is coupled to an intermediary node;

a third current source that is coupled between the first node and the eight node; and

a current mirror that includes a first terminal that is coupled to the fourth node, a second terminal that is coupled to the intermediary node, and a third terminal that is coupled to the signal ground.

6. The apparatus of Claim 1, wherein the amplifier circuit comprises a folded cascode type amplifier.

7. The apparatus of Claim 1, the amplifier circuit comprising:

a first transistor that includes an emitter that is coupled to an eight node, a base that is coupled to the fifth node, and a collector that is coupled to a first intermediary node;

a second transistor that includes an emitter that is coupled to the eight node, a base that is coupled to the sixth node, and a collector that is coupled to another intermediary node;

a third current source that is coupled between the first node and the eight node;

a fourth current source that is coupled between the third node and the first intermediary node;

a fifth current source that is coupled between the third node and the second intermediary node;

a current mirror circuit that is referenced to the signal ground;

a first source follower transistor that includes a source that is coupled to the first intermediary node, a gate that is coupled to a biasing signal, and a drain that is coupled to a first terminal of the current mirror circuit; and

a second source follower transistor that includes a source that is coupled to the second intermediary node, a gate that is coupled to the biasing signal, and a drain that is coupled to a second terminal of the current mirror circuit, wherein the second terminal of the current mirror circuit corresponds to the fourth node.

8. The apparatus of Claim 1, further comprising a compensation capacitor that is coupled between the fourth node and the second node.

9. The apparatus of Claim 1, further comprising a compensation capacitor that is coupled between the fourth node and the third node.

10. The apparatus of Claim 1, wherein the first current source is a cascode current source.

11. The apparatus of Claim 1, the band-gap core comprising:

a first diode circuit that is coupled between the signal ground and a seventh node;

a second diode circuit that is coupled between the signal ground and the sixth node;

a first resistor that is coupled between the fifth node and the seventh node;

a second resistor that is coupled between the second node and the fifth node; and

a third resistor that is coupled between the second node and the sixth node.

12. An apparatus as in Claim 1, further comprising: a switching transistor that is coupled between the local power supply and an output, wherein the switching transistor is arranged to selectively couple power from the local power supply to the output, wherein a voltage associated with the local power supply is perturbed when the switching means is activated.

13. An apparatus as in Claim 1, further comprising:

an control amplifier that is arranged to provide a switching control signal in response to an output signal and the reference signal;

a switching transistor that is coupled between the local power supply and an output, wherein the switching transistor selectively couples power from the local power supply to the output in response to the switching control signal.

14. An apparatus, comprising:

a current source means that is arranged to provide current from a first node to a second node, wherein the first node is associated with a local power supply, and wherein the second node is associated with a reference signal;

a controlled current source means that is arranged to selectively sink current from the second node to a third node in response to a control signal from a fourth node, wherein the third node is associated with a signal ground;

a band-gap core means that is coupled between the second node and the third node, wherein the band-gap core is arranged to provide a first reference signal to a fifth node and a second reference signal to a sixth node; and

an amplifier means, wherein the amplifier means includes a first input that is coupled to the fifth node, a second input that is coupled to the sixth node, and an output that is coupled to the fourth node.

15. An apparatus as in Claim 14, further comprising:

a coupling means that is arranged to couple power from an input supply to the local power supply; and

a switching means that is coupled between the local power supply and an output, wherein the switching means is arranged to selectively couple power from the local power supply to the output, wherein a voltage associated with the local power supply is perturbed when the switching means is activated.

16. An apparatus, comprising:

a first transistor that is arranged to provide a current from a first node to a second node, wherein the first node is associated with a local power supply, and wherein the second node is associated with a reference signal;

a second transistor that is arranged to selectively sink current from the second node to a third node in response to a control signal from a fourth node, wherein the third node is associated with a signal ground;

a band-gap core circuit that is coupled between the second node and the third node, wherein the band-gap core is arranged to provide a first sense signal to a fifth node and a second sense signal to a sixth node; and

an amplifier circuit, wherein the amplifier circuit includes a first input that is coupled to the fifth node, a second input that is coupled to the sixth node, and an output that is coupled to the fourth node.

17. The apparatus of claim 16, further comprising a first cascode transistor that is coupled between the first transistor and the second node.

18. The apparatus of Claim 16,

the band-gap core circuit comprising: a first diode circuit that is coupled between the signal ground and a seventh node, a second diode circuit that is coupled between the signal ground and the sixth node, a first resistor that is coupled between the fifth node and the seventh node, a second resistor that is coupled between the second node and the fifth node, and a third resistor that is coupled between the second node and the sixth node; and

the amplifier circuit comprising: a differential pair circuit, a current mirror circuit, and a third current source, wherein the differential pair circuit includes inputs at the fifth and sixth nodes, a common node at an eight node, and outputs at first and second intermediary nodes, wherein the current source circuit is coupled to the common node, wherein the current mirror circuit is coupled to the first and second intermediary nodes, and wherein the current mirror circuit is referenced to the signal ground.

19. The apparatus of Claim 18, further comprising:

a first cascode transistor that is coupled between the differential pair circuit and the first intermediary node; and

a second cascode transistor that is coupled between the differential pair circuit and the second intermediary node.

20. The apparatus of Claim 19, further comprising:

a first diode connected transistor that is coupled between the common node and a third intermediary node;

a second diode connected transistor that is coupled between the third intermediary node and a fourth intermediary node; and

a fourth current source that is coupled between the fourth intermediary node and the third node, wherein the first diode connected transistor, the second diode connected transistor, and the fourth current source are arranged to operate a sa biasing circuit for the first and second cascode transistors.